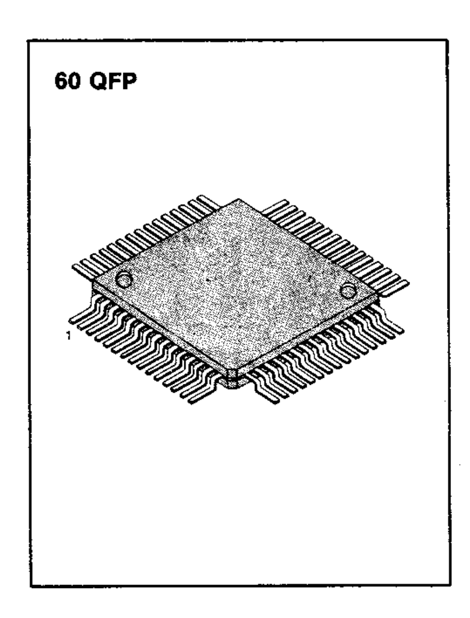
1 CHIP DIGITAL SERVO PROCESSOR FOR VCR

KA8320 is a VCR servo IC that includes analog amps.
And it can use for various head type VCR set.



FUNCTION

- **4 Head switching logic**
- **DAC output by switched capacitor**
- **C-Sync separator**
- **Digital noise rejection**
- **VISS function**
- **DFG, CFG frequency compensation amp**
- **Power On reset (Preventing Overflow)**
- **Frame servo**
- **VISS code write-in and detecting.**

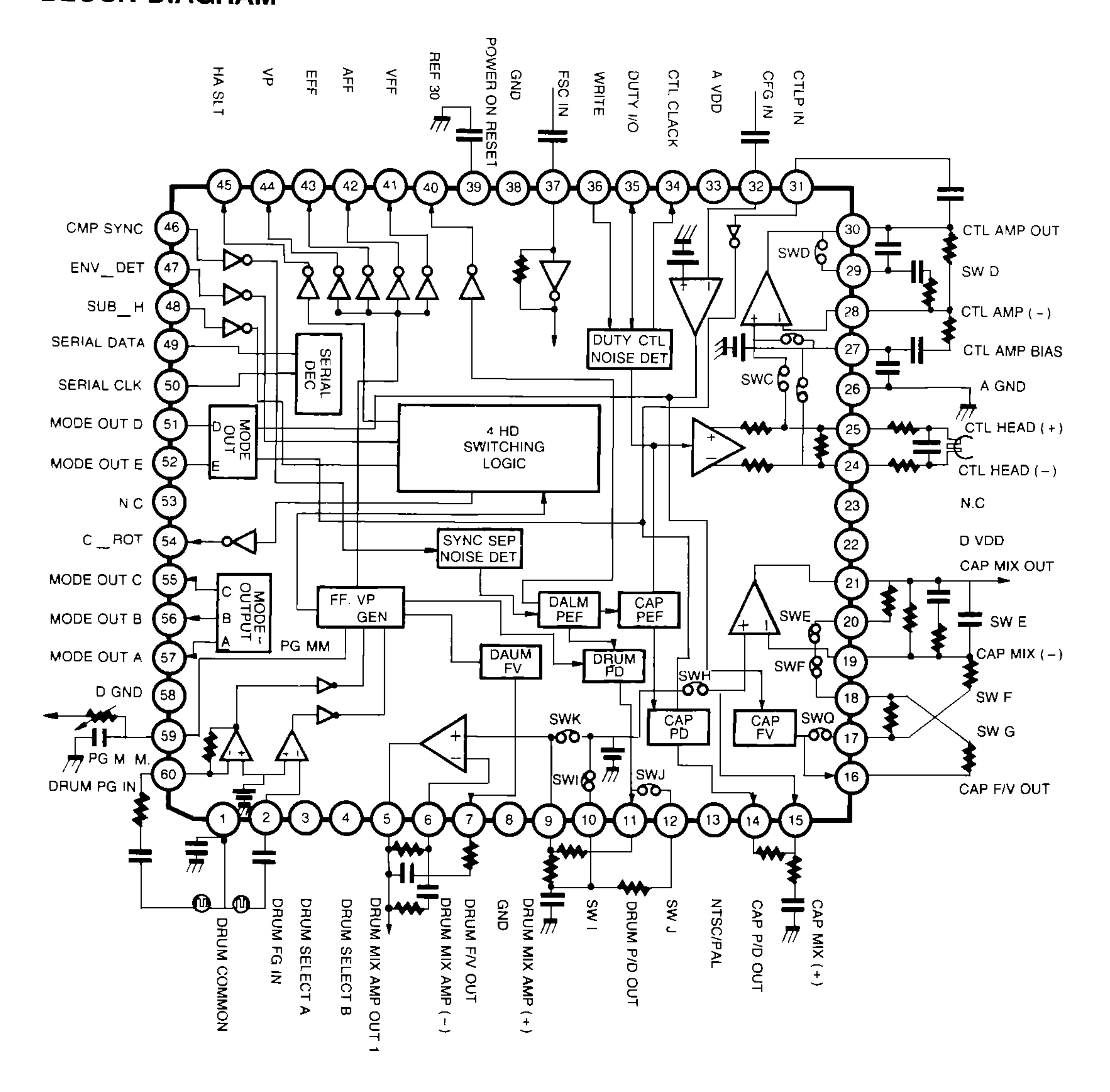
ORDERING INFORMATION

Device	Package	Operating Temperature
KA8320	60QFP	−10 ~ 75°C

FEATURES

- Can be used for 6 kind of various head type.
- Stable DFG, CFG operation by internal limitter amp.
- 70 various search speed available.
- 10 various fine slow speed available
- X distance compensation by 7 bit serial data.
- Tracking control by 7 bit serial data.
- Quasi V-Sync position resetting by serial data.
- Minimizing color vibration and spreading by H-Sync discrete integrating f_H compensation.
- Noise and on H-Sync detecting for ble back screen.
- 3 kind of head switching output.
- Frame memory available.
- Digital noise rejection for analog input stage.
- CFG, CTL pulse count down for 2/4/6 detecting.
- High speed access by non-linear PD out.
- CTL pulse amp that has high frequency characteristics, high gain, high speed rising at power-on.

BLOCK DIAGRAM



PIN DESCRIPTION

PIN NO.	FUNCTION	DESCRIPTION
1	DROM COMMON	COMMON OF DFG/DPG. DC VIAS 2.5V
2	DRUM FG IN	DFG LIMMITER AMP IN
3	DRUM SELECT A	OPEN = "M" (see table below)
4		
5	DRUM MIX AMP OUT	INPUT IMPEDANCE IS BELOW 2KΩ OUTPUT DYNAMIC RANGE 0~5V
6	DRUM MIXX AMP OUT	
9	IN	
15	CADSTAN MIX AMP	
19	IN	
21	CADSTAN MIX OUT	
7	DRUM FV OUT	WITCHED CAPACIOR DA OUT
16	CAPSTAN FV OUT	
11	DRUM PD OUT	SWITCHED CAPACITOR DA OUT
14	CADSTAN PD OUT	
13	NTSC/PAL	H: NTSC L: PAL
24	CTL HEAD –	REC CTL OUT
25	CTL HEAD +	
27	CTL AMP BIAS	OPEN LOOP GAIN NO OSCILLATION OUTPUT DYNAMIC RANGE 0~5V
28	CTL AMP (–)	
30	CTL AMP OUt	
31	CTL PUSE IN	2.5V INTERNAL VIAS
32	CFG IN	
34	CTL CLOC	

B \ A	H	M	L
H	2 HEAD	2 HEAD	2 HEAD
M	DA4	DA4	DA4
L	TEST	TEST	TEST

PIN DESCRIPTION (Continued)

<table>
<tr><th>PIN NO.</th><th>FUNCTION</th><th>DESCRIPTION</th></tr>
<tr><td>35</td><td>DUTY I/O</td><td><table><tr><th></th><th>DUTY MODE</th><th>VISS MODE</th></tr><tr><td>H</td><td>DATA = "0"
DUTY = 60%</td><td>VISS NOT
DETECTED</td></tr><tr><td>L</td><td>DATA = "1"
DUTY = 27%</td><td>VISS
DETECTED</td></tr></table></td></tr>
<tr><td>36</td><td>WRITE</td><td>H: CTL OVERWRITE (PB)
L: NORMAL</td></tr>
<tr><td>37</td><td>f_{SC} IN (3 f_{SC}</td><td>INPUT SENSITIVITY ABOVE 150m $V_{P\text{-}P}$ (f_{SC})
350m $V_{P\text{-}P}$ (3 f_{SC})</td></tr>
<tr><td>39</td><td>POWER ON RESET</td><td>PREVENT COVERENT FLOW TO CTL HEAD
FIN BY RESETTING AT POWER-ON.
YOU MUST ATTACH A 0.01mf CAPACITOR TO GND</td></tr>
<tr><td>40</td><td>REF 30</td><td>SERVO REFERENCE SIGNAL</td></tr>
<tr><td>41</td><td>VFF</td><td>VIDEO HEAD SWITCHING PULSE</td></tr>
<tr><td>42</td><td>AFF</td><td>AUDIO HEAD SWITCHING PULSE</td></tr>
<tr><td>43</td><td>EFF</td><td>EXTRA HEAD SWITCHING PULSE</td></tr>
<tr><td>44</td><td>VP</td><td>QUASI VERTICAL PULSE OUT</td></tr>
<tr><td>45</td><td>HA-SLT</td><td>4 HEAD AMP SELECTING OUT</td></tr>
<tr><td>46</td><td>CMP SYNC</td><td><table><tr><td>BIT</td><td>6 2 1 0</td><td></td></tr><tr><td></td><td>0 1 1 1</td><td>C SYNC INPUT</td></tr><tr><td></td><td>1 1 1 1</td><td>EX-RESET INPUT</td></tr></table></td></tr>
<tr><td>47</td><td>ENV DETECT</td><td>ENVELOPE DETECT IN</td></tr>
<tr><td>48</td><td>SUB-H</td><td>4 HEAD LOGIC SUB INPUT</td></tr>
<tr><td>49</td><td>SERIAL DATA</td><td></td></tr>
<tr><td>50</td><td>SERIAL CLOCK</td><td></td></tr>
<tr><td>51</td><td>MODE D</td><td rowspan="2"><table><tr><td>BIT 3 2 1 0</td><td>D</td><td>E</td></tr><tr><td>0 1 1 1</td><td>CFG C/D</td><td>CTL C/D</td></tr><tr><td>BIT 1 1 1 1</td><td>CFG</td><td>CFG 30</td></tr></table>CFG C/D: CFG COONTED DOWN OUT
CTL C/D: CTL COONTED DOWN OUT
(COUNT DOWN RATIO IS DEPENDS ON SEARCU SPEED)
CFG: 30 CAPSTAN PUASE REFERENCE 30Hz (CFG
COUNTED DOWN OUT)</td></tr>
<tr><td>52</td><td>OUTPUT E</td></tr>
</table>

PIN DESCRIPTION (Continued)

<table>
<tr><th>PIN NO.</th><th>FUNCTION</th><th>DESCRIPTION</th></tr>
<tr><td>54</td><td>C-ROT</td><td>COLOR ROTATION OUT</td></tr>
<tr><td>55</td><td>MODE C OUT</td><td rowspan="3">
<table>
<tr><th>BIT 5 4 2 1 0</th><th>A</th><th>B</th><th>C</th></tr>
<tr><td>0 0 1 1 1</td><td>SP</td><td>SP</td><td>LP</td></tr>
<tr><td>0 1 1 1 1</td><td>SP</td><td>EP</td><td>LP</td></tr>
<tr><td>1 0 1 1 1</td><td>CTL DELAY COUNTER</td><td>H-OSC</td><td>NOISE DET.</td></tr>
<tr><td>1 1 1 1 1</td><td>CAPSTAN PHASE DETECT OUT</td><td>DRUM FG</td><td>DRUM PG</td></tr>
</table>
</td></tr>
<tr><td>56</td><td>MODE B OUT</td></tr>
<tr><td>57</td><td>MODE A OUT</td></tr>
<tr><td>59</td><td>PG M.M.</td><td></td></tr>
<tr><td>60</td><td>DRUM PG IN</td><td></td></tr>
</table>

ABSOLUTE MAXIMUM RATIONGS (Ta = 25°C)

Characteristics	Symbol	Value	Unit
Supply VTG	V_{CCMAX}	6.0	V
Power Dissipation	P_D	500	mW
Operating Temperature	T_{OPR}	−10 ~ 70	°C
Storage Temperature	T_{STG}	−40 ~ 125	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 5V)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{CC}		8.0	30	42	mA
2 Value Output Voltage	V_{OL}	Unload	—	0.0	0.05	V
2 Value Output Voltage	V_{OH}	Unload	4.9	5.0	—	V
2 Value Output Voltage	V_{IL}	Load Current = 2mA	—	0.6	1.2	V
2 Value Output Voltage	V_{IH}	Load Current = 2mA	3.8	4.4	—	V
Pull pu Output Voltage	V_{OL}	Unload	0.0	0.1	0.3	V
Pull up Output Voltage	V_{OH}	Unload	4.9	5.0	—	V
Pull up Output voltage	V_{IL}	Load Current = 2mA	—	0.6	1.2	V
Pull up Resistance	R_H		6.0	9.0	13.0	KΩ
3 Value Output Voltage	V_{OL}	Unload	0.0	0.2	0.4	V
3 Value Output Voltage	V_{OM}	Unload	2.3	2.5	2.8	V
3 Value Output Voltage	V_{OL}	Unload	4.6	4.8	5.0	V
3 Value Output Voltage	V_{IL}	Load Current = 1mt	—	0.6	1.2	V
3 Value Output Voltage	V_{IH}	Load Current = 1mA	3.8	4.4	—	V
3 Value Input Resistance	R_M		6.0	9.0	13.0	KΩ
REC CTL Output Voltage	V_{CTL}	Unload, Potential Pin 29 and Pin 30	4.6	4.8	5.0	V
REC CTL Output Impedance	R_{CTL}	I ≦ 3mA, Add Pin 29 and Pin 30	300	550	1000	Ω
2 Value Input V_{TH}	V_{TH}		1.5	2.5	3.5	V
2 Value Input Pull up R_1	R_{H1}		6.0	9.0	13.0	KΩ
2 Value Input Pull up R_2	R_{H2}		18.5	28.0	42.0	KΩ
3 Value Input V_{TH}	V_{TH1}	L/M V_{TH}	1.0	1.4	1.9	V
3 Value Input V_{TH}	V_{TH2}	M/H V_{TH}	3.1	3.5	4.0	V

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
3 Value Input Voltage	V_M		2.0	2.5	2.9	V
3 Value Input Resistance	R_{M1}		18.5	28.0	42.0	KΩ
3 f_{SC} Input Sensitivity	V $3f_{SC}$		—	—	350	mV_{P-P}
f_{SC} Input Sensitivity			—	—	150	mV_{P-P}
Schmitt Input Voltage 1	V_{IS1}		2.2	2.5	2.8	V
CTLP Schimitt Input V_{TH}	V_{+TH1}	Normal Speed	120	150	180	mV_{OP}
CTLP Schimitt Input V_{TH}	V_{-TH1}	Normal Speed	–180	–150	–120	mV_{OP}
CTLP Schimitt Input V_{TH}	V_{+TH2}	Middle Search Speed	240	300	360	mV_{OP}
CTLP Schimitt Input V_{TH}	V_{-TH2}	Middle Search Speed	–360	–300	–240	mV_{OP}
CTLP Schimitt Input V_{TH}	V_{-TH3}	High Search Speed	–680	–600	–520	mV_{OP}
CTLP Schimitt Input V_{TH}	V_{+TH4}	Viss Detect	850	1000	1150	mV_{OP}
CTLP Schimitt Input V_{TH}	V_{-TH4}	Viss Detect	–1150	–1000	–850	mV_{OP}
Limit AMP Voltage	V_{IS2}		2.2	2.5	2.8	V
Limit AMP Input Sensitivity	V_{LMA}		—	—	10	mV_{P-P}
D.PG Input Voltage 2	V_{IS3}		2.2	2.5	2.8	V
PG Schimitt Input V_{TH}	V_{+TH}		380	480	580	mV_{OP}
PG Schimitt Input V_{TH}	V_{-TH}		140	190	240	mV_{OP}
DPG AMP Feedback R	R_{DP2}		80	100	120	KΩ
DPG AMP Input R	R_{DP1}		8	10	12	KΩ
Analog S/W ON R	R_{ASW}		150	300	500	Ω
Power on Reset Input V_{TH}	V_{43TH}		2.9	3.5	4.1	V
Power on Reset Pull up R	R_{43}		24.0	36.0	52.0	KΩ
Sync Input V_{TH}	V_{50TH}	DC Input	1.5	2.5	3.5	V
Sync Input Voltage	V_{50}		1.8	2.3	2.8	V
Sync Input Sensitivity	V_{SYC}	Duty 10%	150	230	310	mV_{P-P}
Sync Input Impedance	R_{50}		18.5	28.0	42.0	KΩ
M.M. V_{TH}	$V_{TH\ M.M}$		2.2	2.5	2.8	V
CTLP AMP Gain	A_{CTL}	f = 10KHz	57	60	62	dB
CTLP AMP Gain	A_{CTLO}	Open Loop Gain	—	85	—	dB
Drum Add AMP Gain	AD	f = 1KHz	57	60	62	dB
Drum Add AMP Gain	AD_O	Open Loop Gain	—	85	—	dB
CAP. Add AMP Gain	AC	f = 1KHz	57	60	62	dB
GAP. Add AMP Gain	ACO	Open Loop Gain	—	85	—	dB

FUNCTION SPEC

1. DFG

	DFG	COUNTER CLOCK	COUNTER BIT	FV-GAIN	DRUM PD ADJ
NTSC	719 36 Hz	$f_{SC}/2$	11 BIT	60.75 mV/%	596Hz ~ 306Hz
PAL	600.00 Hz	$f_{SC}/3$	11 BIT	60.13 mV/%	496Hz ~ 758Hz

2. DPG

		S/H FREQ.	COUNTER CLOCK	COUNTER BIT	PD GAIN	
					KP 1	KP 2
NTSC	Phase Detect	29.97Hz	$f_{SC}/4$	11 BIT	1.092 V/ms	3.277 V/ms
	f_H Compensation	3.93KHz	$f_{SC}/4$	11 BIT	1.092 V/ms	3.277 V/ms
PAL	Phase Detect	25Hz	$f_{SC}/4$	11 BIT	1.353 V/ms	4.059 V/ms
	f_H Compensation	3.91Hz	$f_{SC}/4$	11 BIT	1.353 V/ms	4.059 V/ms

3. CPG

		S/H FREQ.	COUNTER CLOCK	COUNTER BIT		PD GAIN			
						KP 1		KP 2	
				NORMAL	+6 dB	NORMAL	+6 dB	NORMAL	+6 dB
NTSC		29.97 Hz	$f_{SC}/8$	11 BIT	10 BIT	0.546 V/ms	1.092 V/ms	1.639 V/ms	3.277 V/ms
PAL	PB	25 Hz	$f_{SC}/8$	11 BIT	10 BIT	0.677 V/ms	1.353 V/ms	2.030 V/ms	4.059 V/ms
	REC	25.22Hz							

4. CFG

				CFG FREQ.	S/H FREQ.	COUNTER CLOCK	COUNTER BIT	FV GAIN
NTSC	NORMAL & SEARCH	NORMAL	SP	SEE CAPSTAN F/V CENTER FREQ.	1078.9 Hz	$f_{SC}/2$	11 BIT	40.50 mV/%
			LP		539.6 Hz	$f_{SC}/4$		
			EP		359.6 Hz	$f_{SC}/6$		
		+6 dB	SP		1078.9 Hz	$f_{SC}/2$	10 BIT	81.00 mV/%
			LP		539.5 Hz	$f_{SC}/4$		
			EP		359.6 Hz	$f_{SC}/6$		
	SLOW	SLOW A	SP	809.1 Hz		$f_{SC}/2$	11 BIT	54.00 mV/%
			LP	404.6 Hz		$f_{SC}/4$		54.00 mV/%
			EP	269.7 Hz		$f_{SC}/6$		54.00 mV/%
		SLOW B	SP	581.7 Hz		$f_{SC}/2$	11 BIT	75.12 mV/%
			LP	404.6 Hz		$f_{SC}/4$		54.00 mV/%
			EP	269.7 Hz		$f_{SC}/6$		54.00 mV/%
PAL	NORMAL & SEARCH	NORMAL	SP	SEE CAPSTAN F/V CENTER FREQ.	756.7 Hz	$f_{SC}/4$	11 BIT	35.76 mV/%
			LP		378.4 Hz	$f_{SC}/8$		
		+6 dB	SP		756.7 Hz	$f_{SC}/4$	10 BIT	71.52 mV/%
			LP		378.4 Hz	$f_{SC}/8$		
	SLOW	SLOW A	SP	567.5 Hz		$f_{SC}/4$	11 BIT	47.68 mV/%
			LP	283.7 Hz		$f_{SC}/8$		47.68 mV/%
		SLOW B	SP	378.4 Hz		$f_{SC}/4$	11 BIT	71.52 mV/%
			LP	283.7 Hz		$f_{SC}/8$		47.68 mV/%

5. CAPSTAN FV CENTER FREQUENCY (KHz)

	FORWARD					REVERSE				
SERIAL BIT	NTSC			PAL		NTSC			PAL	
11 10 9 8	SP	LP	EP	SP	LP	SP	LP	EP	SP	LP
0 0 0 0	1.079	0.539	0.360	0.757	0.378	1.079	0.539	0.360	0.757	0.378
0 0 0 1	2.158	1.079	0.719	1.513	0.757	2.158	1.079	0.719	1.513	0.757
0 0 1 0	3.236	1.618	1.079	2.270	1.135	3.236	1.618	1.079	2.270	1.135
0 0 1 1	4.455	2.158	1.438	3.109	1.513	4.138	2.158	1.438	2.921	1.513
0 1 0 0	5.569	2.697	2.517	3.886	1.891	5.174	2.697	2.517	3.651	1.891
0 1 0 1	7.796	3.898	3.236	5.441	2.720	7.242	3.621	3.236	5.111	2.556
0 1 1 0	10.024	5.012	7.796	6.996	3.498	9.312	4.655	7.242	6.572	3.286
0 1 1 1	11.584	5.569	3.712	8.049	3.886	9.988	5.173	3.449	7.092	3.651
1 0 0 0	12.743	12.743	12.743	8.854	8.854	10.986	10.986	10.986	7.801	7.801
1 0 0 1	13.901	13.901	13.515	9.659	9.659	11.985	11.985	11.652	8.510	8.510
1 0 1 0	15.060	15.060	15.060	10.464	10.464	12.984	12.984	12.984	9.219	9.219
1 0 1 1	16.218	7.239	4.826	11.269	5.052	13.983	6.725	4.483	9.928	4.762
1 1 0 0	17.376	8.353	5.569	12.074	5.830	14.981	7.759	5.173	10.637	5.494
1 1 0 1	18.535	9.467	6.311	12.879	6.607	15.980	8.794	5.864	11.346	6.227
1 1 1 0	SLOW									
1 1 1 1	SEE 4. CFG									
CAPSTAN PD ADJ	NTSC −7.2~8.4%					PAL −8.0~9.6%				

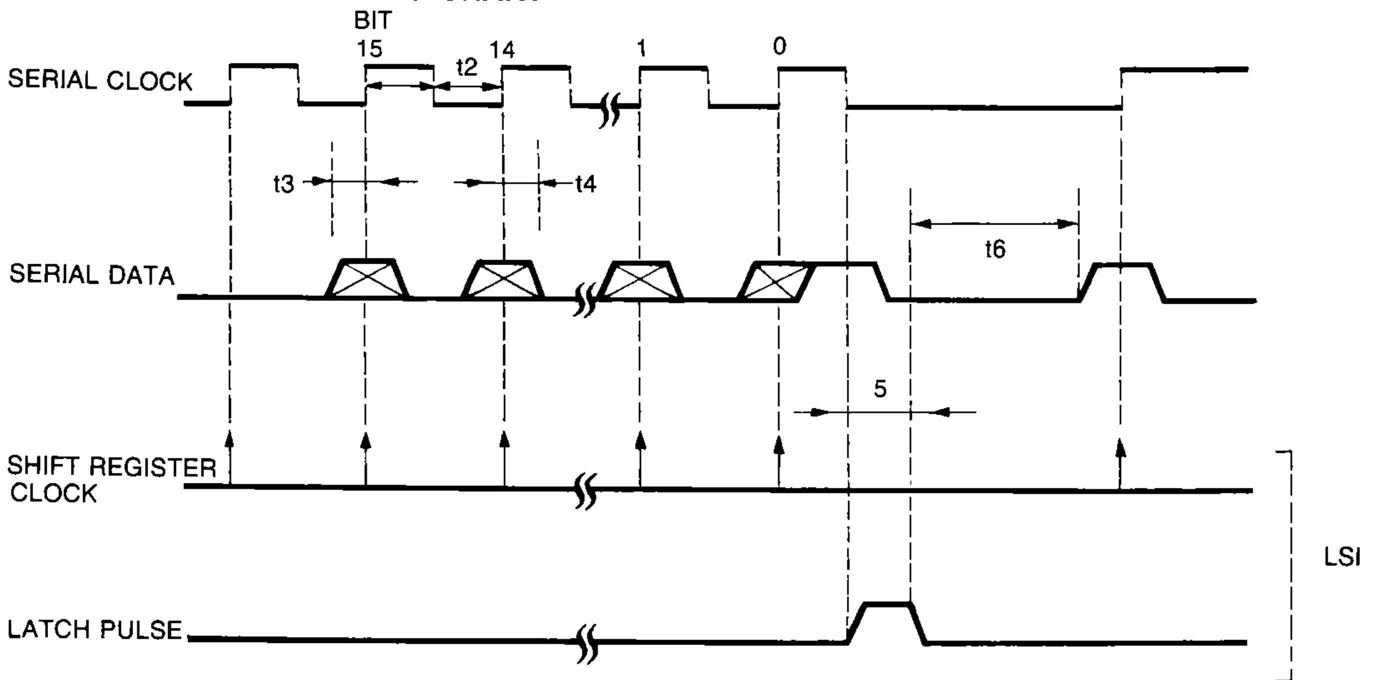
6. CAPSTAN GAIN

SWG	SWF	+6 dB	NTSC SP	NTSC LP	NTSC EP	PAL SP	PAL LP
OFF	OFF	OFF	SLOW	SLOW X1	SLOW X1, 2	SLOW	SLOW X1
ON	OFF	OFF	X1, 2	X2, 3, 4, 5	X3, 4, 7	X1, 2	X2, 3, 4, 5
OFF	ON	OFF	X3, 4	X7, 9	X9, 10, 13	X3, 4	X7, 9
ON	ON	OFF	X5, 7, 9	X10, 13, 15, 17	X15, 17, 21	X5, 7, 9	X10, 13, 15, 17
ON	ON	+6 dB	X10, 11, 12, 13 14, 15, 16	X22, 24, 26	X33, 35, 39	X10, 11, 12, 13 14, 15, 16	X22, 24, 26

7. CTL SCHMITT VTH

VTH	NTSC SP	NTSC LP	NTSC EP	PAL SP	PAL LP
±150 mV ±30 mV	SLOW	SLOW X1	SLOW X1	SLOW	SLOW X1
±300 mV ±60 mV	X1, 2	X2, 3, 4, 5.	X2, 3, 4, 7	X1, 2	X2, 3, 4, 5
±600 mV ±80 mV	X3, 4, 5, 7, 9, 10, 11, 12, 13 14, 15, 16	X7, 9, 10, 13, 15, 17, 22, 24 26	X9, 10, 13, 15, 17, 21, 33, 35 39	X3, 4, 5, 7, 9, 10, 11, 12, 13 14, 15, 16	X7, 9, 10, 13, 15, 17, 22, 24 26
±1000mV ±150 mV	111 MODE D7 = 1				

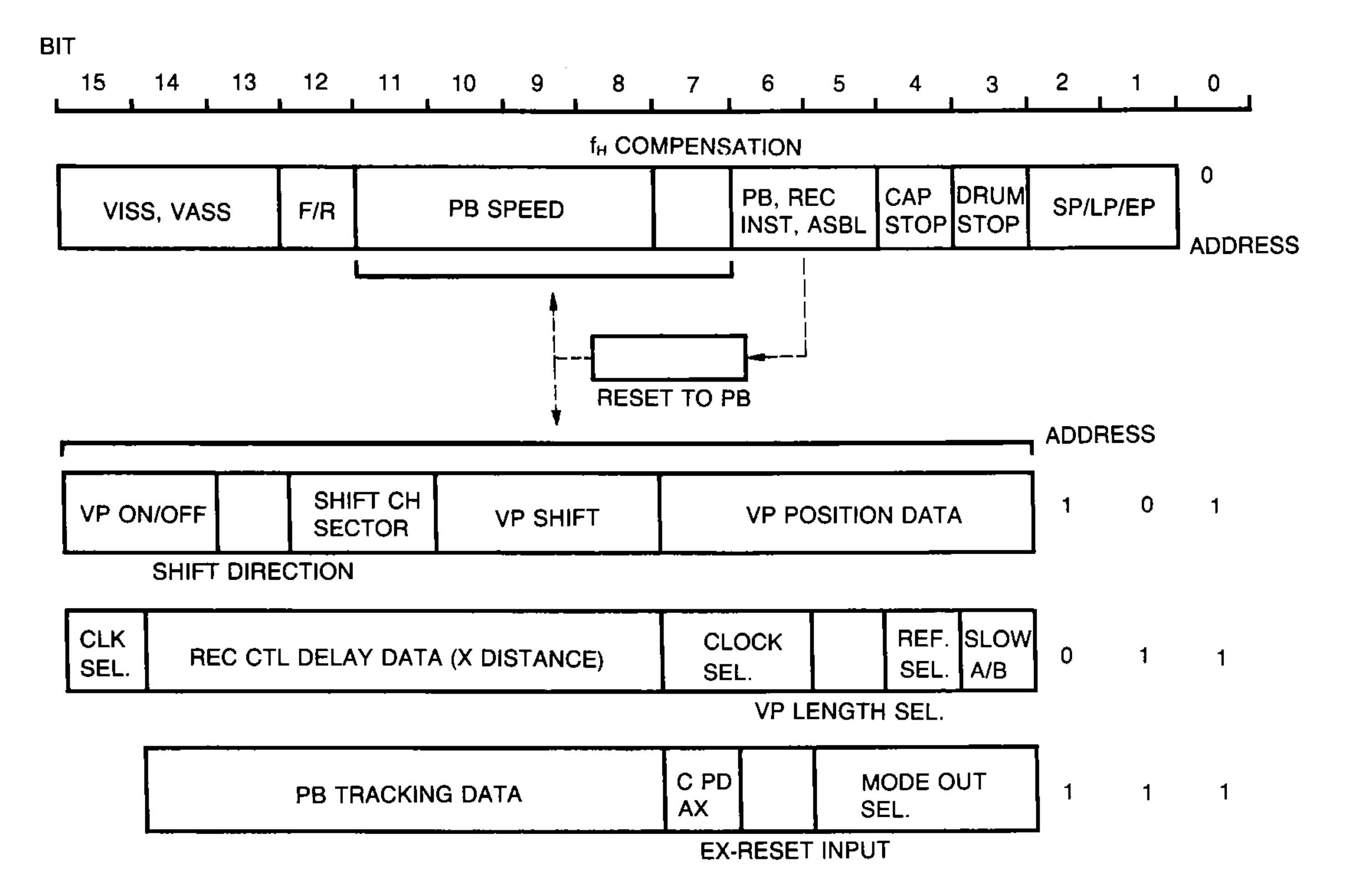
8. SERIAL INPUT TIMING CHART



t1 ≥ 1us, t2 ≥ 1us, t3 ≥ 0.3us, t4 ≥ 0.3us, t5 ≥ 0.5us, t6 ≥ 0.5us

① Previous 16 bit data become valid when serial data become "H" at serial clock negative edge.
② Serial data and clock are "L" state at t6 after data latch and this period must be over 500ns.
③ Serial input is pulled-up by 10KΩ and be careful on tire delay. If you want to increase speed, then add a pull-up resister externally.

9. SERIAL DATA INPUT REGISTER



① KA8320 includes 53 bit register. LSB 2~0 bit is the address of each register.
② AT POWER-ON, whole register presetted.
③ PB speed, f_H compensation, VP control register is resetted automatically when current mode changed into other mode except PB mode.
④ Capstan P/D fixed register is resetted at normal high-speed.

10. SERIAL DATA TABLE 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Notes				
													0	0	0	SP				
													0	1	0	LP				
													1	0	0	EP				
												0			0	DRUM STOP & CAP PD FIX				
												1			0	DRUM ON				
											0				0	CAPSTAN STOP				
											1				0	CAPSTAN ON				
									0	0					0	REC				
									0	1					0	ASBL				
									1	0					0	INST				
									1	1					0	PB				
								0	1	1					0	NOR				
								1	1	1					0	f_H Alignment ON				
																NTSC			PAL	
				0	0	0	0		1	1					0	SP × 1	LP × 1	EP × 1	SP × 1	LP × 1
				0	0	0	1		1	1					0	2	2	2	2	2
				0	0	1	0		1	1					0	3	3	3	3	3
				0	0	1	1		1	1					0	4	4	4	4	4
				0	1	0	0		1	1					0	5	5	7	5	5
				0	1	0	1		1	1					0	7	7	9	7	7
				0	1	1	0		1	1					0	9	9	21	9	9
				0	1	1	1		1	1					0	10	10	10	10	10
				1	0	0	0		1	1					0	11	22	33	11	22
				1	0	0	1		1	1					0	12	24	35	12	24
				1	0	1	0		1	1					0	13	26	39	13	26
				1	0	1	1		1	1					0	14	13	13	14	13
				1	1	0	0		1	1					0	15	15	15	15	15
				1	1	0	1		1	1					0	16	17	17	16	17

10. SERIAL DATA TABLE 1 (Continued)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Notes
				1	1	1	0		1	1					0	SLOW ① CAP P/D FIX
				1	1	1	1		1	1					0	SLOW ② CAP P/D FIX, DRUM P/D FIX
			0												0	FWD
			1												0	REV
0	0	0													0	DUTY DET. MODE
0	0	1													0	DUTY DET. MODE VISS REC FF RESET
0	1	0													0	VISS MODE
0	1	1													0	VISS MODE, VISS REC FF RESET
1	0	0													0	VISS MODE, VISS DET. FF RESET
1	0	1													0	VISS MODE, VISS DET. FF RESET VISS REC FF RESET
1	1	0													0	VISS MODE, VISS WRITE
1	1	1													0	WRITE MODE, VISS REC FF RESET

11. SERIAL DATA TABLE 2

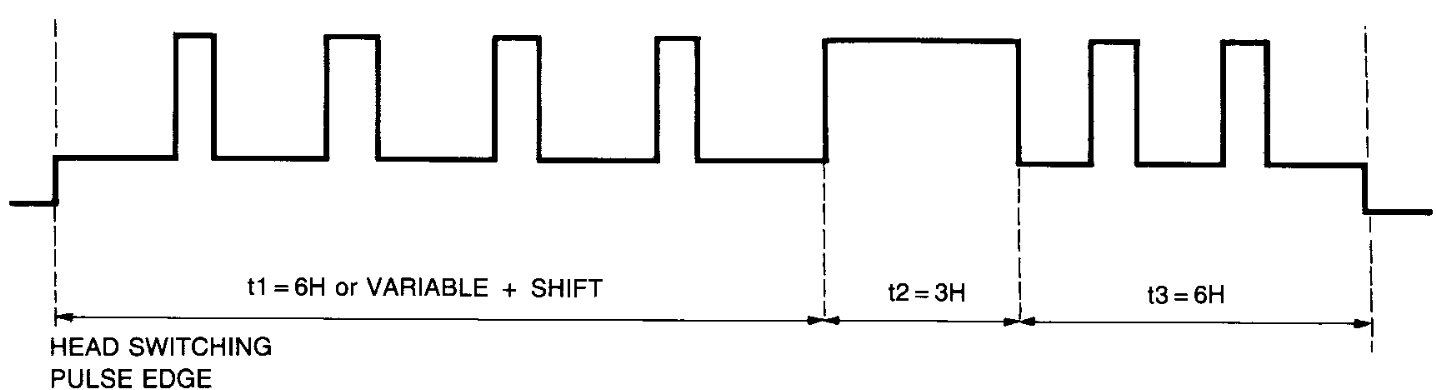
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Notes				
	MSB						LSB													
	*	*	*	*	*	*	*						1	1	1	PB. TRACKING DATA				
																(MODE CTL)				
																A	B	C	D	E
												0	1	1	1				CFG/CD	CTL C/D
												1	1	1	1				CFG	CFG30 (REC)
										0	0		1	1	1	SP	SP	LP		
										0	1		1	1	1	SP	EP	LP		
										1	0		1	1	1	CTL DELAY COUNTER	H-OSC OSC	NOISE DET.		
										1	1		1	1	1	CAP PD	DRUM FG	DRUM PG		
								0					1	1	1	P.CTL SCHMITT 3				
								1					1	1	1	P.CTL SCHMITT ±1000mVop C.P/D				
									0							PIN50 C.SYNC				
									1							PIN50 EX-RESET				
								MSB				LSB								
								*	*	*	*	*	1	0	1	VP POSITION DATA				
					0	0	0						1	0	1	VP SHIFT QUANTITY 0.1H				
					0	0	1						1	0	1	VP SHIFT QUANTITY 0.5H				
					0	1	0						1	0	1	VP SHIFT QUANTITY 1.0H				
					0	1	1						1	0	1	VP SHIFT QUANTITY 1.5H				
					1	0	0						1	0	1	VP SHIFT QUANTITY 2.0H				
					1	0	1						1	0	1	VP SHIFT QUANTITY 2.5H				
																	CH1	CH2		
			0	0									1	0	1	VP SHIFT SELECT	FIX	FIX		
			0	1									1	0	1	VP SHIFT SELECT	FIX	SHIFT		
			1	0									1	0	1	VP SHIFT SELECT	SHIFT	FIX		
			1	1									1	0	1	VP SHIFT SELECT	SHIFT	SHIFT		
		0											1	0	1	VP SHIFT DIRECTION (+)				
		1											1	0	1	VP SHIFT DIRECTION (−)				
0	0												1	0	1	VP OFF (L LEVEL OUTPUT)				
0	1												1	0	1	VP 3 VALUE (M LEVEL OUTPUT)				
1	0												1	0	1	VP ON (3 VALUE OUTPUT)				
1	1												1	0	1	VP MONITOR CUT (H LEVEL OUTPUT)				

12. SERIAL DATA TABLE 3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Notes
	MSB						LSB									
	*	*	*	*	*	*	*						0	1	1	REC CTL DELAY (X VALUE ALIGNMENT)
											0		0	1	1	REF SEL NOR
											1		0	1	1	REF SEL FIELD DET
										0			0	1	1	VP SEL NOR
										1			0	1	1	VP SEL +6H
1								0	0				0	1	1	CLOCK SEL 3 f_{SC}
0								1	1				0	1	1	CLOCK SEL f_{SC}
												0	0	1	1	SLOW A
												1	0	1	1	SLOW B
												0	0	0	1	TEST MODE



13. VERTICAL PULSE



At slow or ×2 play mode, t1 adjusted, else CH1-CH2 VP position would be fixed.

MODE		CH1	CH2
2 HEAD		FIX	FIX
DA-4	SP	FIX	VARYING
	SP	VARYING	FIX

Position adjustment by serial data 5 bit is as follows. while fixed value is about 6.0H.

NTSC	64 (41.5-N)/f_{SC}	3.0H ~ 11.7H
PAL	64 (43.75-N)/f_{SC}	2.9H ~ 9.9H

① **VP SHIFT**

BIT	13	12	11	10	9	8		3	2	1	SHIFT
	—	—	—	0	0	0		1	0	1	0.0 H
				0	0	1					0.5 H
				0	1	0					1.0 H
				0	1	1					1.5 H
				1	0	0					2.0 H
				1	0	1					2.5 H

② **VP SHIFTING CH & SHIFTING DIRECTION**
(⊕○ means delaying direction)

BIT	13	12	11	10	9	8		3	2	1	CH-1	CH-2
	0 / 1	0	0	—				1	0	1	FIX	FIX
	0	0	1	—							FIX	⊕ SHIFT
	1	0	1	—							FIX	⊖ SHIFT
	0	1	0	—							⊕ SHIFT	FIX
	1	1	0	—							⊖ SHIFT	FIX
	0	1	1	—							⊖ SHIFT	⊕ SHIFT
	1	1	1	—							⊕ SHIFT	⊖ SHIFT